analog dialogue

A forum for the exchange of circuits and systems for measurement, control, and test

COMPUTERIZED TEST SYSTEM FOR LINEAR DEVICES (page 3)

Easy to Set Up and Use — Requires No Programming Skills, Tests Amplifiers, A/D and D/A Converters, and Much More

Complete contents on page 3

ANALOG DEVICES

Volume 14, Number 3, 1980

Editor's Notes

TESTING: 1, 2, 3

We tend to eschew flamboyant statements and extravagant claims in these columns, but the headline of one of our recent advertisements made a deep impression on us: "The Most Powerful Benchtop Test System in the World."

These gutsy words, referring to the LTS-2000 test system and the LTS-2010, its BASIC-programmable version, have shock value but are likely to be taken with a grain of salt by today's engineers, inured as they are by exposure since childhood to the hyperbolic claims of advertisers, political candidates, and other seekers of our immediate attention to an often less-than-deserving message.

In this case, after considering the concept, hardware, software, and future outlook for the LTS-2000, we have found the message to be rather close to the mark. What the LTS-2000 provides, in short, starts with the framework of a *universal* tester: precision sources and measuring circuitry, controls, computer, memory, and communication facilities for humans and machines. To this are added specialized hardware and software (for example, family boards, device socketry, and program disks) to test specific classes of devices, and within those classes, specific device types.

Thus, the list of devices it is testing today, already impressive, is but a drop in the bucket when compared to the potential of these machines. *The universal nature of its architecture means that growth of the capabilities of the LTS-2000 family is limited principally by the rate at which software and test peripherals can be developed, and after that, by the growth of the universe of devices to test.*

Because of its potential significance to the broad readership of *Analog Dialogue*, we are going well beyond the brief summary in the last issue. In a series of brief articles, you can learn what it is and what it's like to use it, short of actually laying hands on it. Described here are the System (page 3), the Console (page 4), the Software (page 6), the Family Test Boards (page 8), and actual op amp and DAC test programs—created by users in dialogue with the machine (page 14). ▶

MORE GRIST FOR THE DIALOGUE

The growth of Analog Devices owes much to a strong penchant for investing in and encouraging entrepreneurial ventures, both intramural (e.g., MACSYM) and external (e.g., Nova Devices, subsequently Analog Devices Semiconductor). Our batting average with external ventures has stimulated our appetite for more, to the point that the critical constraint has become the availability of minimally dilutive non-debt capital. As described in more detail elsewhere,* we have devised at least a partial solution to the dilemma through the formation of Analog Devices Enterprises, a mechanism to spread our wings over a broader range of the exciting new developments which are occurring in our industry. This means that you, our readers, can look forward to increasing diversity in the technologies covered by *Analog Dialogue* in future years. ▶

Dan Sheingold

**Analog Devices, inc., 1980 3rd Quarter Report*, available upon request.

THE AUTHORS

Fred Pouliot (page 3), Director of Component Test Systems at Analog Devices, has a BSEE from Northeastern University and has done graduate work, while teaching undergraduate courses. He is a member of both TBII and HKN. After several years of designing analog circuits, he became a marketing specialist, then served as Marketing Manager for various product lines and, most recently, as Division Marketing Manager for Measurement and Control Products (MACSYM).

Al Ryan (pages 3, 4, 5), Senior Staff Engineer for Component Test Systems, has a BSEE from the University of Massachusetts at Amherst. He joined Analog Devices six years ago as Test Engineer for the Semiconductor Division. He was responsible for developing the system concepts and designing much of the hardware of the LTS-2000 and LTS-2010 test systems.

John Chang (page 4), a Project Engineer for the CTS Engineering Group, has a bachelorate from Penn State in electronic design engineering. Previously employed by Inforex and Raytheon, he is at present assigned to Systems Programming and Systems Hardware Design. His current projects include the design of a floating-point hardware board for LTS testers.

Mike Slocombe (page 6) joined CTS as System Software Designer after 5 years in the Analog Devices Semiconductor test-engineering group and a brief stint at LTX. At ADS, he designed computer-based in-house test equipment and helped implement testing of many of the monolithic products on commercial testers. He formerly worked at Raytheon and has attended Northeastern University and the Berklee College of Music.

(More authors on page 18)

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Route 1 Industrial Park, P.O. Box 280, Norwood, Mass. 02062

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COMPUTERIZED TEST SYSTEM FOR LINEAR DEVICES

Easy to Set Up and Use; No Programming Skills Required
Tests Op Amps, A/D and D/A Converters, Regulators, References

by Fred Pouliot and Al Ryan

For more than fifteen years, Analog Devices has been a leading manufacturer of high-precision linear circuits. Besides a superior ability to conceive, design, manufacture, and market such products, a key factor in maintaining our leadership has been the continuing—and growing—capability to create test techniques and equipment. We have attacked and solved many of the problems that occur in high-speed, high-accuracy testing, and have even applied our knowledge and experience to the successful automatic trimming of ICs on the wafer.

In the LTS-2000, these skills are applied to the solution of a related problem faced by *users*: how to test precision linear products manufactured by ourselves and others. The LTS-2000 is a flexible, easy-to-use, benchtop test system which reflects both our testing competence and our successful design and manufacture of measurement-and-control subsystems.*

With the LTS-2000, you can test virtually any component to the manufacturer's own specifications. The growing list includes DACs, ADCs, and linear amplifiers—including op amps, voltage and current regulators, voltage comparators, followers, and similar devices. Future system capabilities are planned to embrace multipliers, dividers, log amps, CMOS switches, and a user-configurable universal family board for use with the BASIC-programmable LTS-2010 in user-proprietary testing.

Much more powerful than a simple tester, the LTS-2000 can be used for basic go/no-go testing, component selection and grading, engineering analysis, qualification testing, and as a diagnostic tool for component evaluation.

Its power and versatility are easy to command through sophisticated software (see page 6). With the prepared test program, the operator just loads the system, inserts the device, and presses the *start test* switch. The LTS-2000 does all the rest. To write your own program is almost as easy, and no programming experience is required: Just fill in the blanks via the keypad, in response to prompts displayed on the System Console (see page 4), with information from the device data sheet. When all the test parameters have been entered, the program is written to the disk and becomes part of your test library. You can change test parameters, reorder tests, and add or delete tests easily and quickly with the system's full editing capability.†

The LTS-2000 Linear Test System comprises the System Console, Family Board Assemblies, Socket Assemblies, and Socket P.C. Boards (see page 8). The *system console* includes a 16-bit microcomputer, a Measurement Section (which provides the control function and performs the final measurements for all devices), a floppy-disk drive, a 20-column thermal strip printer, a 40-character dot-matrix display, a keypad, and function

*For example, MACSYM 2 and MACSYM 20; data upon request.
†If you would like a demonstration of the LTS-2000, use the reply card to request it. Indicate what kinds of devices you are interested in testing. For unlimited flexibility in testing, the *LTS-2010, programmable in BASIC*, is available.

switches, plus ports for RS-232 (2), IEEE-488, and a handler.

The *family-board module*, providing the special functions necessary to test a class of devices (e.g., ADCs, DACs, op amps), is a drawer-like module that slides directly into the System Console. A *socket assembly* is a plugin module which provides the mechanical interface between the Family Board and the DUT. Plugged into the Socket Assembly is the *socket p.c. board*, which contains a socket and any required associated circuitry (e.g., for compensation) for a specific device type.

Other available facilities include a software-controlled automatic-handler interface, an integral statistical analysis package, an NBS-traceable system reference voltage, and test measurement resolutions up to 16 bits. All of this is available at one-quarter of the "big-system" price. For example, complete systems that include a family board and everything needed to test op amps are available for well under $30,000. ▶

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VERSATILE SYSTEM CONSOLE FOR ACCURATE MEASURING

Provides Test Voltages, Computation, Display, Self-Calibration Interfaces with Handlers, Peripherals, IEEE-488, and Human Operators

by Al Ryan and John Chang

The LTS-2000 functions as a microcomputer-controlled stimulus-response system. It supplies power and reference voltages and currents to the device under test (DUT), provides appropriate forcing-function signals and controls to the device, and then measures its response, all under program control. The measurements are converted to digital data, processed, and then compared to operator-defined test limits, which are used to grade and classify the devices according to performance.

The LTS-2000 automatically calibrates itself every hour—and whenever commanded to do so by the user. This self-calibration facility, combined with an internal system accuracy to within 16 bits, enables the LTS-2000 to test ADCs, DACs, and amplifiers to 12-bit accuracy; in addition, devices can be tested for resolutions of up to 16 bits. The overall 16-bit measurement accuracy of the system starts with a temperature-controlled 10-volt reference. Measurements are compared, to 16-bit accuracy, with the output of a software-linearized reference DAC, using an analytic technique employing triple-precision operation of the internal 16-bit microcomputer. The system can be calibrated externally—and traceably to the National Bureau of Standards—by the use of an optional interface board and a Hewlett-Packard 3455A 6 1/2-digit multimeter, which is controlled via the IEEE-488 port.

Figure 1 is a block diagram of the System Console. In it can be seen the 16-bit microcomputer, with 60K of memory, the 92K floppy-disk drive, and the operator's alphanumeric keypad and function switches (for responding to prompting messages appearing on the 40-character display, which also acts as a moveable window on a 127-character message). The two RS-232 interfaces, to external printers and terminals, the IEEE-488 interface to external instrumentation, and the remote-handler interface can also be seen.

The device under test is plugged into its socket; the socket p.c. board is plugged into the socket assembly, which in turn is plugged into the family board module (page 8). The Family Board interfaces with three kinds of entity: the Source Card, which provides programmable voltage or current supplies for the DUT, the Measurement Card, which provides accurate inputs to and performs accurate measurements on the device under test, and a Digital I/O Card, which operates relays and switches for controlling the DUT and monitoring its operation, and for transmitting digital signals to and from the DUT.

COMPUTER AND DIGITAL FACILITIES

For speed and accuracy, the LTS-2000's computer is a board-level Texas Instruments Model TM990-101M1 16-bit microcomputer, which contains 4K bytes of memory for program loading. The CPU's 16-bit processing power is controlled by a powerful minicomputer instruction-set, which includes multiplication and division instructions. System timing is generated by a four-phase 3MHz crystal-stabilized clock, with a real-time facility. Also provided are 15 priority interrupts for the keypad, function switches, floppy-disk drive, and the IEEE-488 interface. The read-write memory is the Texas Instruments TM990-203-23, with 60K bytes of dynamic RAM; memory transfers are in the form of 16-bit parallel data.

The Console Interface Card contains the hardware necessary to interface the operator's alphanumeric keypad, function switches, and display to the system electronics. This card also contains the 92K Intel 8271 floppy-disk controller and the digital interface, which minimizes interference by providing complete isolation between the processor and the measurement section while tests are being performed.

The Peripheral Interface Card contains interface circuitry for

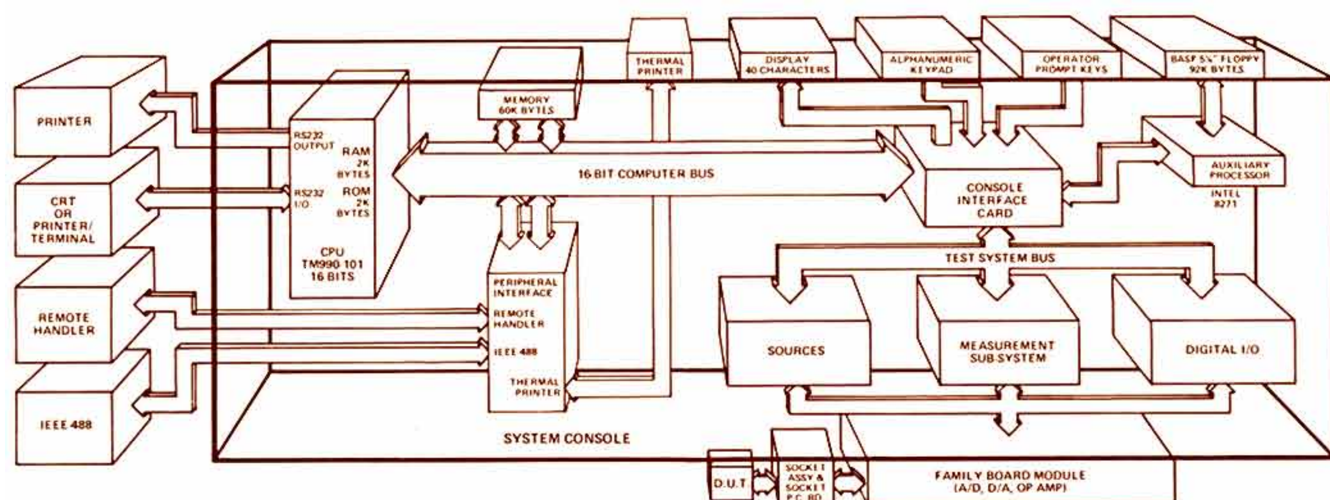


Figure 1. Block diagram of the LTS-2000 test system.

the IEEE-488 data communication and control functions, the remote-handler control, and the system's built-in thermal printer. Outputs to the handler are via relay closures, and inputs from the handler are optically isolated, with threshold levels programmable from 0 to 20 volts. Software controls both the timing and the level of signals. The system temperature alarm is also on this board.

MEASUREMENT SECTION

The Measurement Section of the System Console comprises the Measurement Card, the Source Card, and the Digital I/O Card. They provide, respectively, program-controlled measurement functions, voltage sources and references, and the digital I/O drivers and detectors required for performing device tests. The Measurement Section both controls and performs the actual quantitative measurements for all types of DUTs.

The Measurement Card provides all of the accurate forcing and measurement functions for the LTS-2000. As Figure 2 shows, the card includes the system reference, the system voltmeter circuitry, and a switching network to connect the various references and device-test outputs to the unity-gain precision subtractor in differing combinations and polarities, for direct and null-type measurements. A programmable-gain buffer amplifier, with 64 discrete gains, normalizes the 12-bit ADC input to provide accurate handling of a wide dynamic range of test outputs, from 12V full scale (6mV LSB) to 9mV full-scale (4μV LSB). Accuracy is maintained by hourly automatic system calibration and proprietary software-controlled linearization of the reference-DAC circuit.

The Source Card supplies program-controlled fixed voltages or currents to the device under test via the Family Board. There are two positive 0 to 20V supplies and two negative 0 to 20V supplies, which provide up to plus and minus 150mA respectively, with 0.1V resolution. In addition, a ±10V reference source can provide up to ±10mA with 500μV resolution. Finally, the source card provides ±15V to operate the operational amplifiers that may be used on a given Family Board.

The Digital I/O Card contains the digital drivers and detectors necessary to control the DUT and monitor its operation. It also transmits serial and/or parallel digital data to and from the device under test, as appropriate (e.g., DACs and ADCs). The Digital I/O Card has 24 open-collector drivers (which can each sink up to 200mA) and 24 detectors, with threshold levels programmable from 0 to 10V. In addition, this card provides data-bus signals, 5V power, and digital ground to the Family Board. ▶

SPECIFICATIONS

(typical @ +25°C and 115V, 60Hz operation)

Accuracy: Overall measurement accuracy to better than 16 bits (0.002%)

Examples of Test Specifications:

- Op Amps:
  - Gain-bandwidth products to 100MHz
  - Slew rates to 1000V/μs
  - Input bias currents from 10fA
- Voltage Regulators (Fixed, Adjustable, Positive, Negative, Dual Tracking)
  - Load Current to 15A Pulse
  - Load Regulators to 0.01%/V_{OUT}
- DACs and ADCs:
  - Accuracy to 12 bits
  - Resolution to 16 bits

CPU: TI, TM990-101, 16 bit

Memory: TI, TM990/203, 64Kilobyte RAM

Storage: 5-1/4" floppy disk, 92 Kilobyte capacity

Display: 40-character, dot matrix

Operator Keyboard: 30 alphanumeric keys for data entry
6 fixed function keys
5 programmable function keys with indicator lights

Strip Printer: 20-column, alphanumeric thermal printer

Power Requirements: Selectable, 115V ac or 230V ac 50/60Hz
250 watts.

Dimensions: 19"WX26"DX12"H (48X66X31cm^3)

Weight: 75lb (39kg)

Operating Temperature: +10°C to +40°C

Humidity: Non-condensing

Optional Peripherals

Printer: TI Model 820KSR, 150 char/s, 132 col, 110 to 9600 baud

CRT Terminal: Perkin-Elmer Model 550
12" diagonal screen,
24 lines of 80 characters/line
Full 128 char ASCII, 110 to 9600 baud

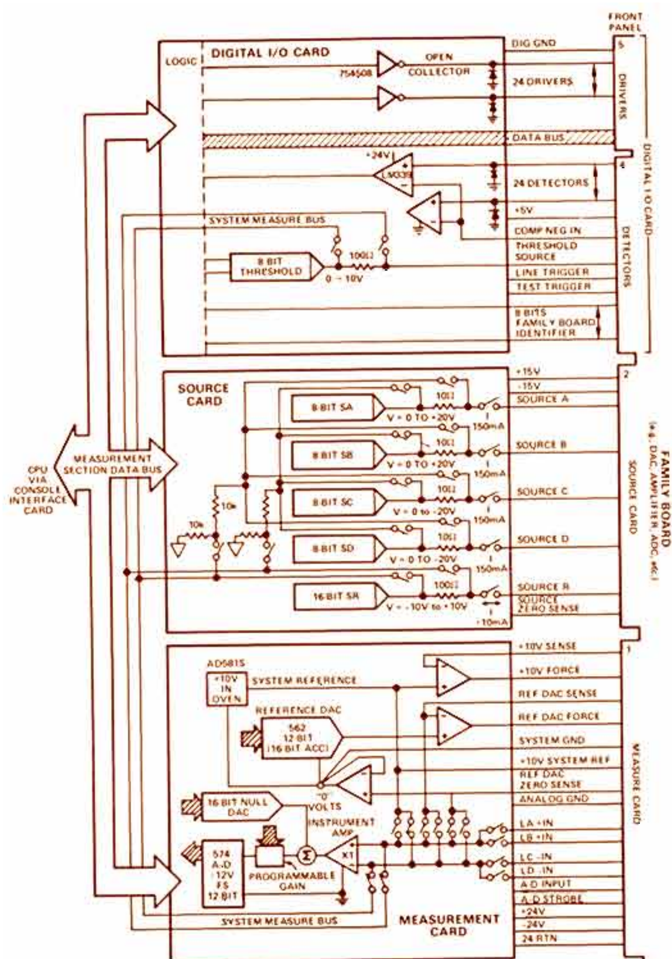


Figure 2. Measurement section, showing measurement, source, and digital I/O cards, with their connections to the family board.

SYSTEM SOFTWARE DESIGNED FOR UNSKILLED OPERATORS

Self-Generated Prompting, Operation, Display, Printout, Statistics
Tests are Easy to Create, Perform, and Interpret, Using Disk Storage

by Mike Slocombe

The system software is designed so that an unskilled operator can run the LTS-2000 efficiently in a short period of time with a minimum of training.* The key to this ease of use is a system of prompts which are displayed on the System Console. The operator needs only to read and respond to the information displayed on the console. (S)he is not required to make any evaluations or judgements or to remember what action to take when a particular test result occurs. The decision mechanisms have been built into the software.

As shown below, there are five function switches located directly beneath the display. When the system requires information or instructions, it will display up to five choices (prompts), each directly above a corresponding function switch.

PROGRAM STORAGE

The LTS-2000 system software includes an Operating System disk, a Create disk, a Family Test disk, and blank discs for storing specific device test programs.

The *operating system* disk is used to initialize the LTS-2000. When the system is first turned on, it will instruct the operator to insert the Operating System disk into the disk drive.

The *create* disk contains the fill-in-the-blanks test menu for a particular class of devices. For example, there are individual Create disks for d/a converters, op amps, etc.

Once a program has been written using the Create disk, it can then be written to a formatted *blank* disk and thus becomes a permanent part of the user's test-program library.

The *family test* disk is used to set up the LTS-2000 to test a particular class of devices, e.g., DACs, op amps, etc. When devices are to be tested, the operator first loads the Operating System, then the Family Test program, and finally the appropriate device-test disk, on which the user-created program has been stored.

TESTING DEVICES

Setup for a typical day's operation takes just a few minutes. First, the user plugs in the appropriate Family Board, Socket Assembly, Socket P.C. Board, and turns the LTS-2000 on. The system will automatically perform a memory check and request that the Operating System be loaded (if there is an anomalous situation in Memory, its location will be displayed). After the operating system has been loaded, the LTS-2000 automatically completes its self-calibration routine (and does so every hour thereafter, and upon request). Again, if there is a malfunction that does not permit calibration to be completed, the location will be displayed. The Family Test program and the prepared test program for the specific device are then loaded, and the LTS-2000 is ready for testing.

To begin testing, the user inserts the device into the socket and presses the Start Test switch. When the tests are completed, if the device has passed them all, the display indicates:

PASS, BIN 1

or a similar message, and an audible tone is sounded. The user removes the device, places it in the appropriate bin, and inserts the next device.

If a device has failed some tests, the display may indicate:

FAIL, BIN 3

and a different audible tone is sounded. The device is removed and placed in Bin 3. The procedure is repeated for each device.

At the end of the test lot or group, press the DISPLAY key and the system will display the following prompts:

DLOG	SETUP	STAT	YIELD	DEBUG
F1	F2	F3	F4	F5

If a summary of the yields is desired, press Function Switch F4, directly below the YIELD option, and two prompts will be displayed:

PRINT	CLEAR			
F1	F2	F3	F4	F5

If F1 is depressed, the LTS-2000's strip printer will record a summary of the test data. If F2 is pressed, the yield counters will be cleared and another test run may be initiated.

As the prompts indicate, the LTS-2000 also provides other formats for data outputs, including data logs (DLOG) and statistical analysis (STAT). Other output devices are optionally available, including external printers and terminals. To select the desired format, the user presses the DISPLAY switch and then presses the appropriate Function Switch directly beneath the displayed choice.

Data log (DLOG) records the results of individual tests in the program and is often useful in isolating the reason a device failed. There is complete flexibility in selecting the devices and tests to be data-logged, and as to which output means is used.

*Unlimited flexibility in testing is available for the more-sophisticated in the *BASIC-programmable LTS-2010*.

Statistical analysis (STAT) makes it possible for the user to collect data on certain tests and to display that data in cumulative, histogram, and/or graphical form. STAT is particularly useful in characterizing new devices and detecting trends in familiar devices.

Summary sheet (YIELD) provides a convenient way of determining how well a group of devices fared in testing. It includes such information as test program name, date and time, number of devices tested, number (and %) of devices in each classification ("Bin"), number of times each test was failed (and % to total number of devices tested).

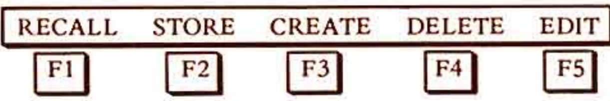
CREATING TEST PROGRAMS

New device test programs can be created in minutes with the Create program disks and the device manufacturer's data sheet or a specification-control drawing. The clear, easy-to-follow prompts displayed on the System Console guide the operator through the complete menu of these fill-in-the-blanks programs. The number of tests and the order in which they can be performed can be selected to establish a test program tailored to suit a specific need or application. This is a typical procedure:

Turn the LTS-2000 on and load the Operating System. When the system indicates

remove the Operating System disk, insert the Create program disk for the type of device to be tested, and press Function Switch F5. A message will appear. For example,

will be displayed; it indicates, in this case, that the digital-to-analog converter Create program is loaded. Press the Start Test switch (directly beneath the five Function Switches), and the LTS-2000 will request a program name; it is entered via the alphanumeric keypad (e.g., DAC 80-CBI-V). The system will then prompt:



Press Function Switch F3, directly under the word CREATE; by displaying the first of a series of prompts, the system starts to configure the LTS-2000 for the type of device to be tested.

For example, if the LTS-2000 is to be configured for testing a specific digital-to-analog converter type, the following is a partial listing of the prompts that will appear. The user responds by an entry from the alphanumeric keypad.

NUMBER OF BITS? *12 (carriage return)*
POS OR NEG TRUE LOGIC (P/N) ? N
CODE TYPE? *BIN (carriage return)*
SERIAL OR PARALLEL DATA (S/P)? P
.
.
.
ANY LOGIC OUTPUTS? (Y/N) N
DEVICE WARMUP TIME (S) *10*

When all of the prompts that configure the system have been answered, the system displays another set of prompts for defining the test options. Each test can be selected or eliminated by typing Y (yes) or N (no). This is a partial list of the test options for the DAC test program:

TEST: UNIPOLAR ZERO (Y/N) ? N
TEST: FULL SCALE (Y/N) ? N
TEST: REFERENCE VOLTAGE (Y/N) ? N
TEST: BIPOLAR ZERO (Y/N) ? N
TEST: BIPOLAR + FULL SCALE (Y/N) ? N
TEST: BIPOLAR - FULL SCALE (Y/N) ? N
TEST: VSA SUPPLY CURRENT (Y/N) ? N
.
.
.
TEST: LOGIC 1 BIT CURRENT (Y/N) ? N
TEST: LOGIC 0 BIT CURRENT (Y/N) ? N
TEST: VSA SUPPLY REJECTION (Y/N) ? N
TEST: VSB SUPPLY REJECTION (Y/N) ? N
TEST: VSC SUPPLY REJECTION (Y/N) ? N
TEST: VSD SUPPLY REJECTION (Y/N) ? N

If *Y* is the response for any test, a series of prompts is displayed, one at a time, defining the hardware for that test.

For example, if the response to the first question is *Y*,

TEST: UNIPOLAR ZERO (Y/N) ? Y
(TEST #1) CHANGE SOURCE VOLTAGES (Y/N) ? N
CONNECT 1K LOAD (Y/N) ? N
CHANGE RELAY DRIVE CODE (Y/N) ? N
INPUT LOGIC ARRAY (Y/N) ? N
REPEAT HARDWARE QUESTIONS (Y/N) ?

When the test list is completed, the LTS-2000 prompts

END OF PROGRAM (Y/N) ?

If the response is *N*, the entire test list is repeated, and the test conditions can be changed. Tests can be added to the end of the program, inserted anywhere in the program, deleted, or modified using the EDIT program. If the response is *Y*, the system displays:

The program can be saved on a disk having enough capacity. If it is to be saved on a blank disk, the Create disk is removed, a blank formatted disk is inserted, and Function Switch F2 is pressed. The disk, which can hold as many as 32 test programs, can then become part of a permanent test-program library. Some typical test programs can be found on pages 14-16.

AMPLIFIER TESTING

The Op Amp Create program is used in much the same way as the DAC Create program. After the Op Amp Create program is loaded and Function Switch F3 under the CREATE prompt is pressed, the following series of prompts is displayed to aid in configuring the LTS-2000 for testing op amps:

PROGRAM NAME: *(e.g., TEST AD741K carriage return)*
NUMBER OF SECTIONS (1, 2, 3 or 4)? *1*
V_S+ (INITIAL) VOLTS? *+ 15 (carriage return)*
V_S- (INITIAL) VOLTS? *- 15 (carriage return)*
DEVICE WARMUP TIMES(S) *5*
NUMBER OF STROBES/MEAS?

After these questions have been answered, the next series to be displayed defines the test options. As in the case of DACs, each test can be selected or eliminated by the response *Y* (yes) or *N* (no). Up to 40 tests are available in the op-amp create-a-test program, and they include supply current, offset voltage and current, bias currents, gain, common-mode and power-supply rejection, bandwidth, slew rate, channel separation, output range and short-circuit current, and balance range, for a variety of supply voltages, load resistances, etc.

Like DAC-testing programs, amplifier programs can be transferred to disk for permanent retention; they can also be debugged (in Debug, the operator can stop the program at a predetermined point, leaving the system set up as programmed—a useful function when determining why a device is not being tested as planned and where the problem lies). An amplifier program can be seen in pages 14-16. ▶

LTS-2000 Linear Test System

SOFTWARE-CONFIGURED FAMILY BOARDS SPEED TESTING

Interchangeable Boards Test Op Amps, DACs, ADCs, etc.

by Gary Sheehan, Jan Johnson, and Tim Wilhelm

The primary control functions and the final measurements common to all types or classes of devices are to be found in the System Console. The *family board modules* provide stimuli, gains, and special functions needed to exercise and test a particular group or class of linear devices. Typical families represented by family boards include operational amplifiers, digital-to-analog converters, and analog-to-digital converters. These drawer-like modules slide directly into the System Console at bottom front.

DAC FAMILY BOARD MODULE

The DAC Family Board Module performs all functions necessary to test DACs of up to 16-bit resolution. It will test voltage-output or current-switching DACs, DACs with or without buffer registers, and serial-input or parallel DACs.

To test a 12-bit DAC for accuracy to within 1/2 least-significant bit requires a measurement capable of resolving errors of the order of 0.01%. This in turn calls for comparisons to considerably greater accuracy. The LTS-2000 performs these measurements by comparing the output of the device under test and a 16-bit-accurate reference DAC. The inevitable errors introduced by offsets and scale factors in the Family Board are compensated for by software; the reading that is calculated and datalogged automatically takes all of the above factors into account.

The DAC Family Board Module allows both voltage- and current-output DACs to be tested. If a current-output DAC without internal span resistors is tested, the LTS-2000's current-to-voltage converter (Figure 1) converts and scales full-scale output to a voltage at the 10V level; this permits the measurements to be normalized. Full-scale output of voltage-output DACs, with the various choices of internal span resistors, is similarly normalized, using a voltage amplifier.

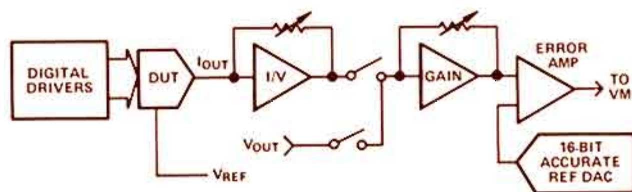


Figure 1. DAC family board functional block diagram.

The normalized 10-V signals are compared to the 16-bit accurate reference DAC in an error amplifier, and the amplified error signal is read by the system's voltmeter. Devices which require an external reference are provided with a 16-bit-accurate reference voltage of the proper polarity (see also Figure 2, page 5) for the test.

DAC MEASUREMENTS

Offset in a unipolar DAC is measured with all device bits off. The measurements of the device under test (DUT) are compared on the DAC Family Board with those of the theoretical device. The error signal is amplified and read by the system voltmeter. In bipolar DACs, with offset binary or 2s complement coding, offset can be measured both at the all-bits-off ($-V_{REF}$) point and at bipolar zero.

Gain. To measure gain, all device bits are turned on, and the output of the device is measured. The offset measurement is subtracted from this reading to obtain full-scale span, and the LTS-2000 calculates the deviation from ideal full scale. The system also calculates the value of the least-significant bit (LSB) for correction of gain and comparisons of step size in linearity testing.

Nonlinearity or Relative Accuracy. Rather than exercise every possible code—a costly and time-consuming process—the LTS-2000 performs three kinds of test to characterize the most common manifestations of error: *bit errors, summation errors, and carry errors.* After calibrating the end points (*offset* and *gain*), and storing the span measurement and deriving the value of the LSB (Span/(2^n−1)), the LTS-2000 exercises each bit in turn, starting with the MSB, by turning it on, with all other bits off. The output with the MSB on is compared with $2^{(n-1)}$ LSB, the output for Bit 2 is compared with $2^{(n-2)}$ LSB, etc., for all *n* bits, and the resulting errors are recorded, in fractions of 1 LSB (e.g., 0.8). These are the *bit errors*, and they are measured in response to one of the program steps. If any bit error is greater than the programmed limit (chosen by the user), the test is failed. Magnitudes and polarities of these errors are recorded.

Another test is for *summation errors*. All bit values having positive errors are summed, all bit values with negative errors are summed, and the sums are compared against preset limits.* The LTS-2000 can perform the test in two ways: by simply summing the bit errors mathematically, and/or by allowing the DUT to perform the summation when all the positive-error or negative-error bits are applied, and comparing the output with the expected value of output, based on the accurately known LSB. The latter method can find *integral nonlinearities* due to the departure from linear superposition in the DUT at those codes. Table 1 shows an example of this technique.

The third test is for *carry errors*, which are a measure of *differential nonlinearity*, since the largest differential nonlinearities tend to occur at carries. When a given bit is zero, followed by all ones (e.g., for Bit 3, 000111111111), and the code is switched to the next step: one followed by all zeros (001000000000), the difference between the output values represented by the two codes should be exactly 1 LSB. Any departure from 1 LSB is a carry error. The technique used by the LTS-2000 to measure carry errors is to null out one of the two adjacent values, measure the difference (actual size of the

*The codes at which these individual sums occur have the largest errors. For any other code, errors of the opposite polarity will be summed and reduce the overall error.

step), and compare it with the accurately known LSB. Carry error is measured for all bits (e.g., from 0111. . .11-to-1000 . . .00 down to 000. . .00-to-000. . .01).

TABLE 1. EXAMPLE OF DAC SUMMATION ERROR.

Suppose that the measured bit errors are as follows (units of 1 LSB)

Bit 1 (MSB)	-0.27
Bit 2	+0.23
Bit 3	-0.03
Bit 4	+0.15
Bit 5	+0.08
Bit 6 through 12	0.00

The sum of the positive errors is +0.46, occurring at 01011XXXXXXX (X = 1 or 0). The sum of the negative errors is -0.30, occurring at 10100XXXXXXX. At any other code, the error will be less; for example, it is +0.16 at 11111XXXXXXX. If the errors are summed algebraically, as above, the summation errors will be less than 0.5 LSB. However, if the codes 01011XXXXXXX and 10100XXXXXXX are actually applied to the DAC and the errors at those codes are measured, it is likely that the actual summation will differ from the algebraic summation error. For example, one might measure errors of +0.52 and -0.27 at those codes, a cause for rejection at the 1/2 LSB accuracy level.

Power-Supply Rejection. Power-supply rejection is measured by the ratio of a change in device output to full scale in response to a change in the power-supply voltage. Testing for this parameter is performed by digitally changing the appropriate supply voltage(s), measuring the output voltage change, calculateing the ratio, and displaying it in either per cent or ppm of full scale per volt of change. Four digitally controlled 0 to 20V device power supplies, two positive (VSA and VSB) and two negative (VSC and VSD), are available for these tests.

Logic Bit Currents. The logic bit-currents are measured for both 1 and 0 inputs. For these measurements, the logic bit currents flow through resistors of known value on the DAC family board. The voltage developed across a resistor is buffered by a data amplifier and measured by the system voltmeter, and the current is computed by Ohm's law. The data is displayed in microamperes.

Device Supply Currents. Supply currents of the device, from each supply used, are measured in the same way as the bit currents, with all bits on (for worst-case measurement). The results are displayed in milliamperes.

Table 2 provides a summary of the salient characteristics of

TABLE 2. DAC FAMILY BOARD MODULE—CHARACTERISTICS.

Device characteristics	
Voltage-output DACs	1V to 100V F.S.
Current-output DACs	1mA to 10mA F.S.
Internal or external reference	±10V range
Internal or furnished span resistors	1, 2, 5, 10kΩ furnished
Unipolar or bipolar output	
coding—positive or negative true	Binary, Offset binary, 2s complement*
Mating socket-assembly module	
10 Test points	+ and -15V (for auxiliary op amps) Analog ground, ground sense, Reference DAC output Instrumentation amplifier output Buffer output, Device output voltage Bit-current-measurement output Logic threshold output
Loads for current-output DACs	1kΩ available on board or connected by user at socket adapter board
System 10V reference	Force and sense connection to compensate for voltage drops
Digital connections	
Digital driver bits (DDB), 16 available	Drive DUT logic inputs 0 to +20V, positive true, 130Ω, 0 to 1mA
Digital control bits (DCB), 8 available	Drive for external relays or logic 0 to +20V, negative true, 10Ω Open collector, sink up to 200mA
Digital readback bits (DRB)	0 to +20V, positive true Threshold accuracy ±0.05V

* BCD available soon

the LTS-2300 D/A Converter Family Board Module. With currently available software, it is capable of testing the vast majority of DAC types; and the software library is continually expanding to extend its repertoire of types and tests.

OP-AMP FAMILY BOARD MODULE

With the Operational Amplifier Family Board Module, the LTS-2000 is capable of performing both static and dynamic tests, including offset voltage and current, bias current, trim range, common-mode and power-supply rejection, output swing and short-circuit current, open-loop gain, slewing rate, gain-bandwidth product, and channel separation (in multi-amplifier devices).

The family board provides the software-configured test circuitry; the basic circuit is shown in Figure 2. In it can be seen all the elements that are used in performing the various tests we shall describe. The key to performance of the tests is the servo loop employing a high-gain integrator with very low offset. Since it is the basic control element in the loop (the "real op amp"), the parameters of the device under test (DUT) can be explored in what amounts to open-loop operation. Here's how the system works:

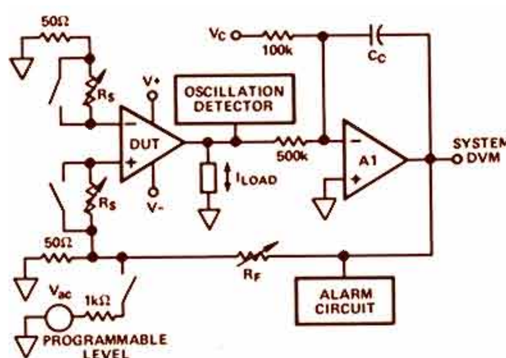


Figure 2. Basic op-amp test circuit.

In the steady-state condition, no current can flow through the integrating capacitor (otherwise the output of A1 would change). Therefore, the currents through the 100kΩ and 500kΩ resistors are equal and opposite, and the output of the DUT is forced to be equal to $-5V_C$, irrespective of the inputs of or components connected to the DUT. The input to the DUT is forced by A1 and the input circuitry to whatever value of input will produce the required output established by V_C.

For example, if $V_C = 0$, the output of the DUT is zero; hence the input to the DUT must be equal to the offset voltage, if the switches across resistors RS are closed to minimize the effect of bias current. Since the input to the DUT is established by A1's output and the resistive divider, R_F and 50Ω, the output of A1 must come to rest at an amplified version of the offset voltage, i.e., $(1 + R_F/50\Omega)V_{OS}$. This output is measured by the system DVM, scaled by software, and recorded.

As Figure 2 shows, provisions are included for the user to connect loads to the DUT's output terminals, for ac input signals and adjustable supply voltages, as well as for detecting oscillation at the DUT output or an open-loop condition that leads to saturation of the integrator output.

OPERATIONAL AMPLIFIER TESTING

Amplifiers are tested by switching appropriate circuit elements in or out, adjusting circuit parameter values, and making suit-

able measurements. In the diagrams associated with the tests, the circuits will be presented in "bare-bones" fashion, with just the elements needed for the test shown. It is worthwhile to keep in mind, though, that each such circuit is a variation of the circuit of Figure 2.

Input Offset Voltage. The input offset voltage, V_{OS}, defined as the voltage required in series with the input to drive the output to zero, is measured in the manner discussed in the example above (Figure 3).

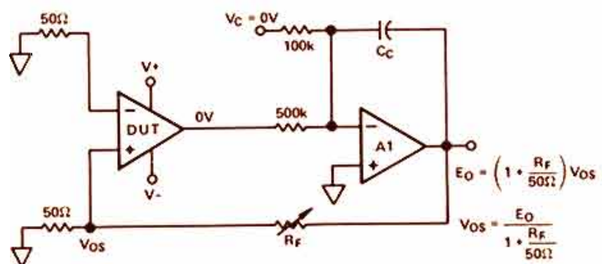
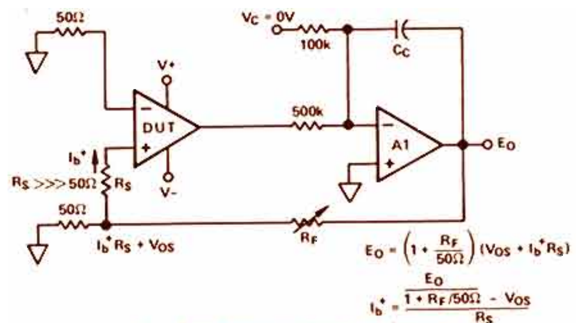
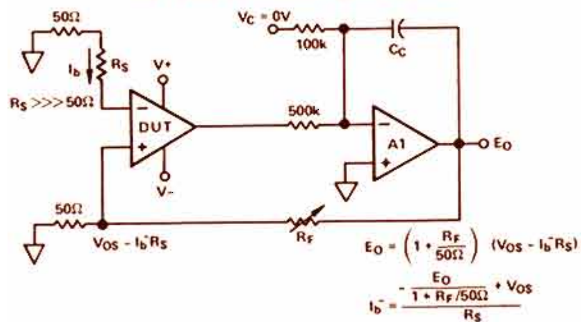


Figure 3. Measuring offset voltage.

Input Bias Current. Input bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero. As Figure 4 shows, input bias current is measured by forcing the bias current to flow through an appropriately large resistor, R_S. When V_C is set to zero, the output of A1 must be whatever voltage is required to bring the output of the DUT to zero, in this case, $(I_b^+R_S + V_{OS})(1 + R_F/50\Omega)$ for the plus (noninverting) input or $(-I_b^-R_S + V_{OS})(1 + R_F/50\Omega)$ for the minus (inverting) input. The output is measured, scaled, and the previously measured V_{OS} is subtracted out, giving the voltage drop across R_S. The computer performs the division, records the correct value of I_b^+ or I_b^-, and makes any necessary comparison to accept or reject the device.



4a. Bias current at plus input.



4b. Bias current at minus input.

Figure 4. Measuring bias current.

Input offset current. Input offset current, I_{OS}, is defined as the difference between the two bias currents at the input, when the output of the DUT is at a null. It is measured by leaving both R_S resistances in the circuit and thus measuring the difference between the voltages developed by the bias currents as the flow through the resistances. The computation is identical to that for bias current (Figure 5).

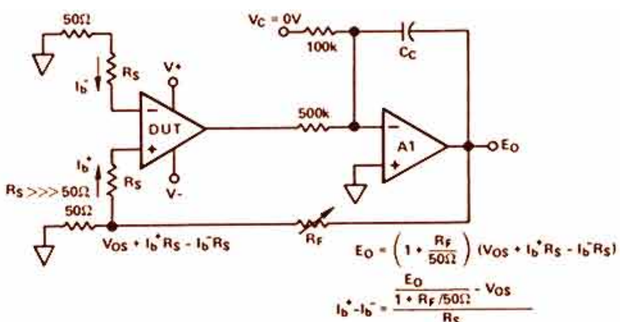


Figure 5. Measuring offset current.

Input offset voltage trim range. This test verifies that, with the recommended trim circuit, the amplifier can be zeroed. The appropriate value of resistance to simulate the trim potentiometer is connected between the trim terminals (Figure 6), and relays connect one or the other of the trim terminals to the specified supply, while the amplifier is connected in the V_{OS} test configuration. If the output of A1 changes polarity (indicating that some intermediate pot setting is capable of zeroing the amplifier), the DUT passes.

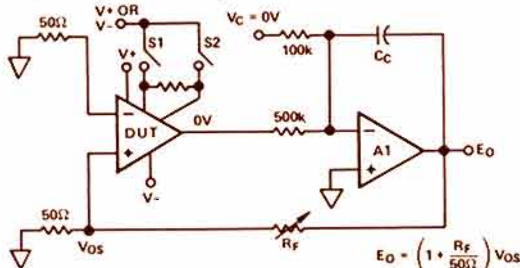


Figure 6. Testing for adequate offset trim range.

Slew(ing) Rate. Slewing rate (usually volts per microsecond) may be defined as the limiting rate of change of output voltage in response to a large input step change. Figure 7 shows a simplified test circuit, and the associated waveforms, for measurement of slewing rate. The measurement technique is basically straightforward: to measure the time required for the voltage to pass between a lower and an upper threshold, and compute the ratio of ΔV to Δt.

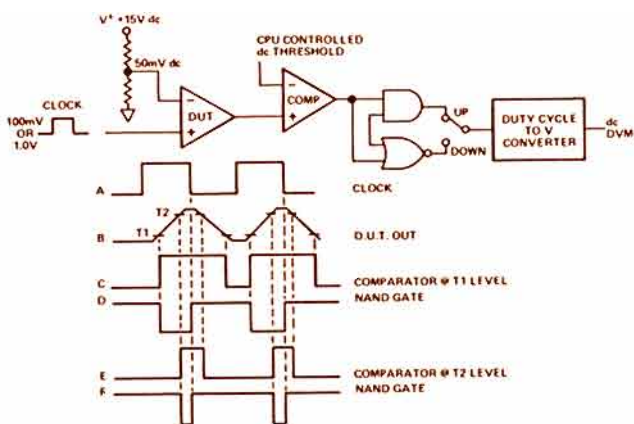


Figure 7. Testing open-loop slew rate of DUT. NAND-gate waveforms are for positive-going swing, NOR-gate waveforms (not shown) for negative swing.

The step is applied as a square wave (A), derived from a crystal-controlled clock. A choice among 16 binary frequencies permits selection of optimum ranges of duty cycle during test for

particular DUT types. The device under test tries to follow the step change but cannot do so immediately (B). As the output rises, it crosses the lower threshold value (T1) and causes a comparator transition to occur (C). The comparator output is NAND-ed with the clock pulse to produce a waveform (D) with duty cycle (% of time high) a function of T1. The duty cycle is measured as an average dc level over a large number of clock cyles.

The threshold is then changed to T2, and the waveforms corresponding to C and D become E and F. Again the duty cycle is measured. Since the difference of the duty cycles is proportional to the time in flight from T1 to T2, the computer determines the slew rate by dividing the difference between the threshold levels, $T_2 - T_1$, by the difference between the duty cycles, with appropriate scaling for frequency. The NOR gate is used instead of the NAND gate when measuring the *descending* slew rate.

Gain-Bandwidth Product. Gain-bandwidth product is defined as the frequency at which the open-loop gain would become unity (0dB), if the amplifier had a single-pole rolloff (i.e., -20dB/decade gain slope). Figure 8 shows the circuit used for the measurement.

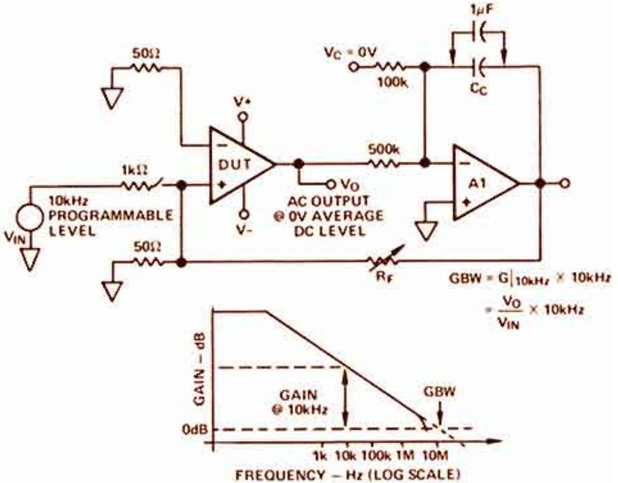


Figure 8. Measuring gain-bandwidth product.

The test loop is closed through integrator A1 (using a large value of feedback capacitance), in order to keep the DUT output at zero dc level. Since the integrator has negligible throughput at high frequencies, the DUT is effectively in an open-loop condition for the high-frequency test signal. The output of a 10kHz ac signal source with programmable amplitude is applied at the + input, via a 1kΩ-50Ω divider, and the output amplitude of the DUT is measured; from this measurement, the open-loop gain at 10kHz can be computed and multiplied by 10kHz to compute the gain-bandwidth product.

Common-Mode Rejection Ratio. Common-mode rejection

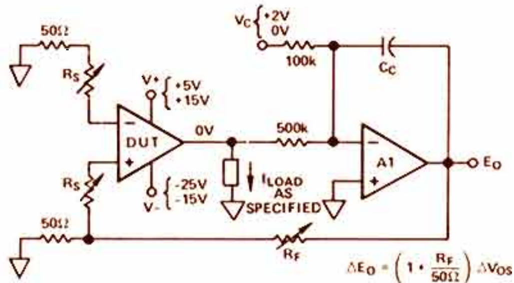


Figure 9. Measuring common-mode rejection.

ratio (CMRR) is defined as the ratio of a change in common-mode voltage to the change in V_{OS} that results. It can be expressed logarithmically in dB: CMR = 20 $\log_{10}$ (CMRR). To test for CMRR, the LTS-2000 raises all sources above their nominal values by the value of the common-mode voltage, then lowers them below nominal by the same amount. This method avoids the use of the precisely matched resistors that are required in a commonly employed technique. Figure 9 shows how the scheme works.

To apply a common-mode voltage of +10V, V+ is changed from +15V to +5V, V- is changed from -15V to -25V, and V_C is changed from 0 to +2V, so that the DUT output changes from 0V to -10V. Thus, common ("ground") is left high-and-dry at +10V with respect to the voltages appearing at the other terminals of the device. The value of V_{OS} under these conditions is measured and stored.

Next, the voltage supplies are set to their nominal values, and V_C is set to zero. V_{OS} is again measured and compared to the previous value. If this 10V common-mode change produces a 0.002V change of V_{OS}, the CMRR is 5000, and CMR is 74dB. For negative CMV swings, the supplies are raised by 10V and -2V is applied at V_C. The resistances labeled "R_S" are used when source resistance or source unbalance is specified.

Power-Supply Rejection Ratio. Power-supply rejection ratio (PSRR) is defined as the ratio of a specified change of power-supply voltage to the resulting change in V_{OS}. To measure PSRR, the LTS-2000 measures and records the value of V_{OS} with normal power-supply levels. The supply voltages are then changed by the specified amount and polarity, and the resulting value of V_{OS} is recorded. The ratio of ΔV_{OS} to the programmed power-supply change is the inverse of the PSRR (µV/V). In the LTS-2010, the logarithm may be computed to provide PSR in dB.

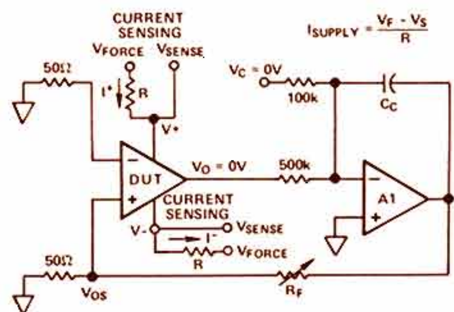


Figure 10. Measuring power-supply currents.

Power-Supply Currents. Power-supply currents are defined as the currents drawn by the DUT from V+ and V-. To measure the current drain, the DUT is connected in a feedback loop (Figure 10), and resistors in series with the supplies provide voltage drops for measuring the currents. Because the output of the DUT is at zero, and a current load is not connected, the load current is essentially zero. The voltage drops are measured and scaled to compute current.

Output Voltage Swing. Output swing is defined as the maximum voltage available at the device output with a given load. Figure 11 shows how output swing is measured. The output is programmed to swing to a large value of voltage (theoretically -50V, for V_C = +10V). The amplifier will swing to saturation at the lowest negative voltage of which it is capable. Similarly, for V_C = -10V, the amplifier will swing to positive saturation.

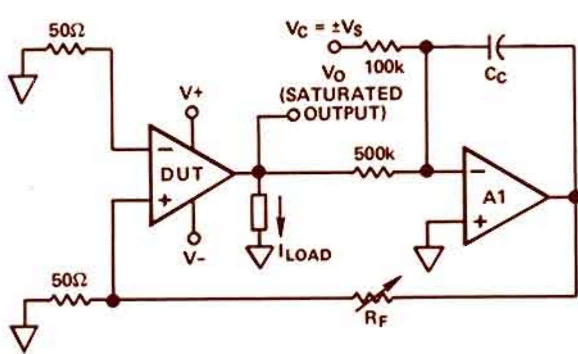


Figure 11. Output voltage swing.

The device output is measured. In the case shown, the load is a user-furnished resistor.

Output Short-Circuit Current. Output short-circuit current (I_{SC}) is defined as an output current limit which will not be exceeded if the output is short-circuited or otherwise overloaded. As Figure 12 shows, the DUT is connected in a feedback loop with its output connected to a user-specified voltage, V_{SENSE} (e.g., 0V). The amplifier will seek to drive the short-circuit to the voltage programmed by V_C—unsuccessfully. Its output current is measured by the system ($I_{SC} = (V_{FORCE} - V_{SENSE})/R$).

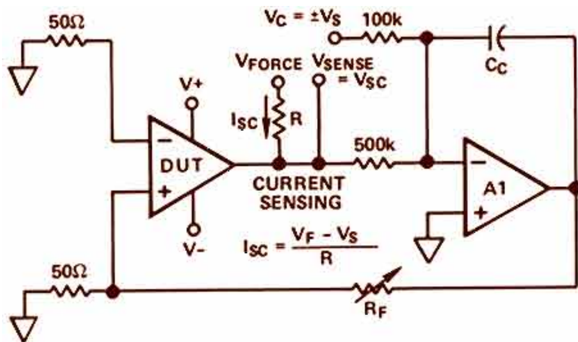


Figure 12. Measuring short-circuit current.

Open-Loop DC Gain. Open-loop gain is defined as the ratio of a change in output voltage to the input voltage change required to produce it. To test for open loop gain (Figure 13) for an output swing from -10V to +10V with a programmed value of load, the power supplies are set to the nominal values. Then V_C is set to -2V, resulting in an output of +10V; the output of the integrator, which is $(1 + R_F/50\Omega)$ times the change in input voltage, is measured and recorded. V_C is set to +2V, driving the DUT output to -10V; the integrator output is again measured and recorded. The difference between the two values of amplifier input is computed and divided into the 20V output change to compute the gain.

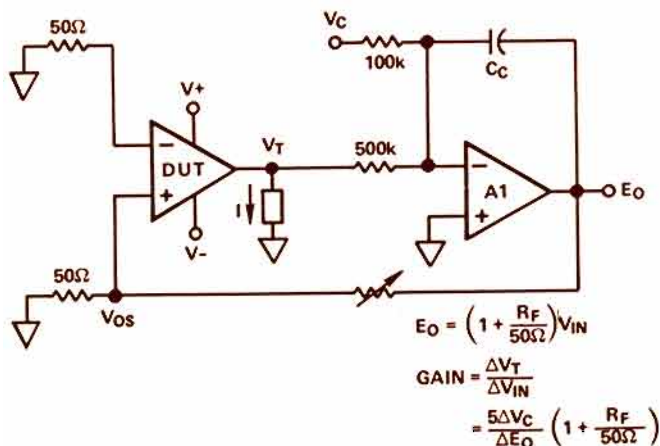


Figure 13. Measuring open-loop gain.

Channel Separation. Channel-separation ratio (in multi-amplifier chips) is the ratio of change in the output voltage of a driven channel to the resulting change in effective input voltage of another channel. To measure channel separation in a dual op amp (Figure 14), one of the units (amplifier B here) is configured in a standard feedback test loop and driven with an ac sine wave at the level required to swing the output 10V peak-to-peak. Op amp A is configured as a unity-gain follower with the input grounded. The ac output of op-amp A is measured. The ratio of the output amplitudes of A and B is a measure of the channel separation.

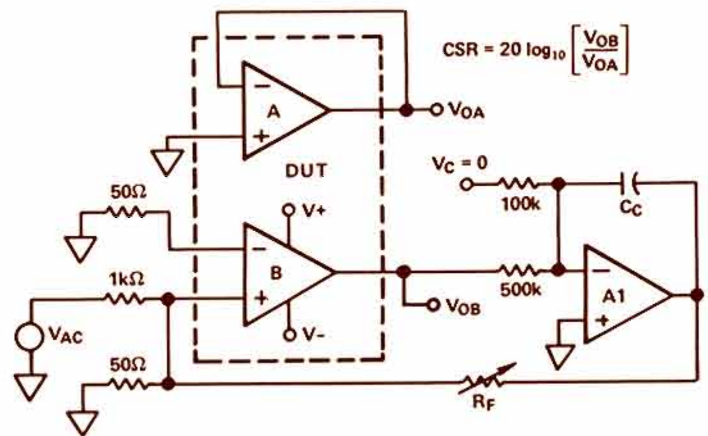


Figure 14. Measuring channel separation in a dual op amp.

Table 3 is a summary of the tests performed by the LTS-2000, using the op-amp family board, and their typical accuracies.

TABLE 3. OP-AMP TEST SPECIFICATIONS

(Typical at 25°C and 115V 60Hz line)

DC PARAMETERS		
Input offset voltage	10μV to 500mV	±(0.2% + 10μV)
Input bias current	10nA to 500μA	±(0.3% + 1nA)
(Note 1)	10fA to 1nA	±(2% + 5fA)
Input offset current	1nA to 500μA	±(0.4% + 2nA)
(Note 1)	10fA to 1nA	±(3% + 10fA)
Supply current, V+, V-	100μA to 50mA	±(0.2% + 10μA)
Output short-circuit current	100μA to 50mA	±(0.2% + 10μA)
Open-loop gain	10 to 1 X 10^6V/V	±(0.25% + 0.1dB)
Power-supply rejection	0.1V/V to 1μV/V	±(0.25% + 0.1dB)
Common-mode rejection	20dB to 120dB	±(0.25% + 0.1dB)
Output voltage swing	100mV to 50V	±(0.4% + 1mV)
Offset-voltage adjustment range	Pass/Fail	±(0.2% + 10μV)
Channel separation	40dB to 120dB	±(5% + 0.1dB)
AC PARAMETERS		
Gain-bandwidth product (Note 2)	100kHz to 100MHz	±(10% + 10kHz)
Slewing rate	0.01V/μs to 1000V/μs	±(10% + 0.001μs)
Channel separation	40dB to 120dB	±(5% +0.1dB)
OPERATING CONDITIONS		
V+ supply	0 to 50V (50mA max)	±0.2V
V- supply	0 to -50V (-50mA max)	±0.2V
Input resistors	50Ω, 1kΩ, 10kΩ, 100kΩ	±0.1%
Input capacitor	0.001μF	±1%
DUT output load impedance	User-supplied	

Notes:
1. Requires Teflon socket, low-leakage relays, high source impedance
2. Assumption: device under test has 20dB/decade linear rolloff

SOCKET ASSEMBLIES

Socket Assemblies are plugin modules consisting of a Socket, a Socket Printed-Circuit Card, and an Assembly Housing. The Socket Assembly provides a mechanical interface between the Family Board Module and the device being tested. Besides performing the primary function of matching the pinout and physical arrangement of leads on the device to the connections of the Family Board Module, the Socket Assembly may also be wired with accessory items, such as relays or LED/switches, to aid the operator in special applications. Socket Assemblies are provided to go with each of the Family-Board Module types; they are currently available for op amps, d/a converters, and a/d converters.

AUTOMATIC HANDLER APPLICATIONS

When the LTS-2000 is used with an automatic component handler, the Family Board is located remotely on the handler unit instead of in the system console. The connections between the Family Board and the Console are made via an Automatic Handler Module, which is plugged into the Family-Board Slot. The analog connections are made via a carefully shielded cable, for minimum interference; current-carrying leads which must transmit accurately determined voltages use remote sensing. All digital connections are opto-isolated, and power for remote digital functions is provided by a dc-to-dc converter, so that there are no galvanic connections between the Console and the remote test system's digital circuitry.

In addition to the functions normally provided via the Family Board Module, a special Remote Handler Interface at the back of the Console provides for communication with the handler. Fourteen functions are provided, including Start-Test Input, Retest Input, Test-in-Process, End-of-Test, Retest Output, 8 Sorts, and Handler Ground. The inputs and outputs are under program control; they can be either positive or negative true, and either pulses or levels. Timing between signals and debouncing are also under software control, to allow the LTS-2000 to interface with the majority of presently available handlers with modifications only to software, instead of hardware.

The eight Sort signals can be programmed as a single 8-bit word, which can be decoded into as many as 255 different outputs. The system can receive and/or generate a *retest* signal (a feature of some handlers that causes the handler to retain the device for another test, rather than automatically sequencing to the next part). The LTS-2000 adjusts summary sheets and parts counts to take the retest into account.

The input signals from the handler can range from +1V to +40V, with a threshold voltage adjustable from 0 to 20V. The outputs are relay contacts connected to handler ground; they can accommodate 0V to 100V (open), 0 to 0.5A, 10W max, protected by 10Ω series limiting resistance.

DEBUGGING

Among other important test functions provided by the LTS-2000 is a Debug function. This permits the operator to stop the program at a predetermined point, while leaving the system setup unaltered. It is especially useful for determining why a device is not testing as expected and where the problem lies. It also permits measurements to be made at the DUT socket.

A/D CONVERTER TESTING

One of the methods used for testing ADCs on the LTS-2000's A/D Converter Family Board is illustrated in Figure 15. Code widths are measured by computing the difference between the average dc levels of triangular waves dithering about the two adjacent code transitions. Here is how it is done:

First, consider the various elements in the loop. The reference DAC establishes the input voltage corresponding to a given code. The integrator generates a ramp that is either positive- or negative-going, depending on the position of the switch, controlled by the output of the digital comparator. The ramp is attenuated and summed with the DAC output, producing a slowly changing input to the ADC under test. The output of the ADC is compared with the code under test (CUT) in a digital comparator, and the polarity of the error determines the polarity of current applied to the integrator. Because the digital comparator is actually a slave microprocessor, the a/d test system is quite flexible and is capable of implementing any of the test methods and handling formats from straight binary coding to 3 1/2-digit seven-segment decoded outputs used by display ADCs.

Suppose that the output of the ADC is low, i.e., A<B. The negative current, $-I_{IN}$, is applied to the integrator, and its output, V_D, increases, thus increasing the input to the ADC. On the next conversion, the test is again performed, and V_D continues to ramp upward until A≥B. At that time, the current into the integrator is reversed, the input to the DUT is reduced, and on a succeeding conversion, A will once again be less than B. The cycle repeats, and a triangular wave will be produced. The servo is now locked into a limit cycle, and V_D will ramp slowly about the transition between CUT and (CUT − 1 LSB). The average level at the output of the integrator is measured (E_1).

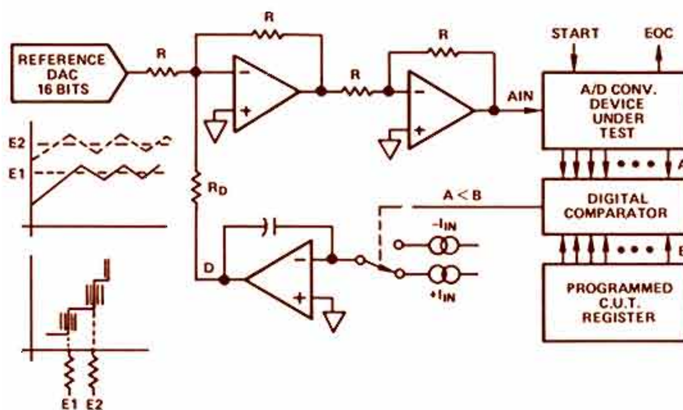


Figure 15. A/D converter testing.

Then, the code under test is set at (CUT + 1 LSB). The same process will occur, resulting in a triangular wave about the transition between CUT and (CUT + 1 LSB). The average level of the integrator output is again measured (E_2). The difference between these levels, $E_2 - E_1$, is proportional to the code width.

By accurately relating the voltage at D to the output of the precision reference, the midpoints of the codes can be checked. Missing codes can be identified by (1) a codewidth measurement of 0 and (2) the skip in the ADC output for a small change of input and continual oscillation between two non-adjacent code values. ◘

SAMPLE PROGRAMS FOR TESTING OP AMP AND DAC

Annotated Programs Show Prompts and Responses
Bin-Elimination Grading System Facilitates Automatic Handling

by Steve Castelli

Two complete LTS-2000 test programs are shown here, with annotations to provide what little explanation is necessary. On this page, we reproduce a program to test a 741-type operational amplifier for supply current, offset voltage, and offset current.

At the completion of the tests, two good grades of device will have been identified. As we have indicated earlier, many other tests and their variations could have been written; this set is kept simple for the sake of clarity.

The first test is for positive supply current with ±15V supplies. If the supply current is less than 1mA or greater than 2.8mA, the device will be rejected. In the second test, the upper limit will be increased to 3.3mA. Any device, rejected by the first test, which falls within the second set of limits is accepted for the second grade.

In the third and fourth tests, the same current limits are applied to the negative supply current, with the same criteria for acceptance and rejection for the two grades.

The 5th test is for V_{OS} with 50Ω input source resistance. If V_{OS} is outside the band ±2mV, the device will be rejected. In the 6th test, the upper limit is increased to ±3mV. A device which has been rejected by the first test but falls within the second set of limits will be accepted for the second grade.

In tests 7 and 8, offset current is tested, using 100kΩ source resistors. The limits in test 7 are ±0.01μA and in test 8 are ±0.05μA. As before, there are two grades of good devices.

After these tests have been performed, the program ends. It could be repeated, amended, added to, stored, or wiped. There are many more tests that could be added, such as open-loop gain, slewing rate, short-circuit current, etc., as listed on an earlier page, where the test circuits are described.

TEST PROGRAM FOR 741J/K

Program	Annotation
PROGRAM NAME ? 741J/K	*In answer to query "Program name", type 741J/K or any name with up to 11 alphanumeric characters*
RECALL STORE CREATE DELETE	*Push button under CREATE*
NUMBER OF SECTIONS (1,2,3 OR 4) ? 1	*Single or multiple device?*
VS+ (INITIAL) VOLTS ? +18 VS- (INITIAL) VOLTS ? -18	*Initial supply voltages for warmup*
DEVICE WARMUP TIME (S) ? .2	*0.2s warmup time*
NUMBER OF STROBES/MEAS ? 1	*Just one repetition (more are possible for noisy signals)*
DEFINE GOOD BINS: 1,2	*Two categories of good device (see next page)*
(TEST : 1) +ICC (Y/N)? Y	*Yes – first test will be for positive supply current*
CHANGE SUPPLY VOLTAGE (Y/N)? Y VS+ = + 18 CHANGE TO +15 VS- = - 18 CHANGE TO -15	*Supply voltages changed to ±15V*
COMMON MODE VOLTAGE (Y/N)? N	*CMV = 0*
LOW LIMIT IN MA = 1.0 HIGH LIMIT IN MA = 2.8	*Limits for acceptable device*
ELIMINATE BINS ? 1	*Failed device must be in either Bin 2 or Bin 3 (or higher)*
REPEAT TEST (Y/N)? N REPEAT TEST WITH VARIATIONS (Y/N)? Y	*Repeat the test, with one or more changes*
(TEST : 2) +ICC (Y/N)? Y	*Yes, test for positive supply current*
CHANGE SUPPLY VOLTAGE (Y/N)? N COMMON MODE VOLTAGE (Y/N)? N	*No change*
LOW LIMIT IN MA = 1.0 HIGH LIMIT IN MA = 3.3	*Leave lower limit at 1.0mA, upper limit at 3.3mA*
ELIMINATE BINS ? 1,2	*Failed device to Bin 3 (or higher)*
REPEAT TEST (Y/N)? N REPEAT TEST WITH VARIATIONS (Y/N)? N	*OK – no more $+I_{CC}$ tests*
END OF PROGRAM (Y/N)? N	*Continue testing*
(TEST : 3) -ICC (Y/N)? Y	*Yes – test negative supply current*
CHANGE SUPPLY VOLTAGE (Y/N)? N COMMON MODE VOLTAGE (Y/N)? N	*No change*
LOW LIMIT IN MA = -2.8 HIGH LIMIT IN MA = -1.0	*Limits for acceptable device*
ELIMINATE BINS ? 1	*Bin 1 if it passes, unless some previous test has eliminated Bin 1*
REPEAT TEST (Y/N)? N REPEAT TEST WITH VARIATIONS (Y/N)? Y	*Repeat test with 1 or more changes*
(TEST : 4) -ICC (Y/N)? Y	*Yes, test for negative supply current*
CHANGE SUPPLY VOLTAGE (Y/N)? N COMMON MODE VOLTAGE (Y/N)? N	*No change*

Program dialogue	Comment
LOW LIMIT IN MA = -3.3	New limits
HIGH LIMIT IN MA = -1.0	
ELIMINATE BINS ? 1,2	Failures to Bin 3
REPEAT TEST (Y/N)? N	
REPEAT TEST WITH VARIATIONS (Y/N)? N	*Finished I_{CC}- test, but not program*
END OF PROGRAM (Y/N)? N	
(TEST : 5) VOS 50 OHM (Y/N)? Y	*Yes, V_{OS} test with 50Ω source resistance*
CHANGE SUPPLY VOLTAGE (Y/N)? N	*No change*
COMMON MODE VOLTAGE (Y/N)? N	
LOW LIMIT IN MV = -2.0	*Offset voltage test limits*
HIGH LIMIT IN MV = 2.0	
ELIMINATE BINS ? 1	*Failed unit cannot reside in Bin 1*
REPEAT TEST (Y/N)? N	
REPEAT TEST WITH VARIATIONS (Y/N)? Y	*Repeat test with changes*
(TEST : 6) VOS 50 OHM (Y/N)? Y	*Yes, V_{OS} test with 50Ω source resistance*
CHANGE SUPPLY VOLTAGE (Y/N)? N	*No change*
COMMON MODE VOLTAGE (Y/N)? N	
LOW LIMIT IN MV = -3.0	*New limits*
HIGH LIMIT IN MV = 3.0	
ELIMINATE BINS ? 1,2	*Failed units must be in Bin 3 (or higher)*
REPEAT TEST (Y/N)? N	
REPEAT TEST WITH VARIATIONS (Y/N)? N	*Finished V_{OS} test (50Ω) but not program*
END OF PROGRAM (Y/N)? N	
(TEST : 7) VOS RS (Y/N)? N	*V_{OS} with some other value of R_S? No.*
END OF PROGRAM (Y/N)? N	*Continue to suggest tests*
(TEST : 7) IOS (Y/N)? Y	*Test I_{OS}? – Yes*
CHANGE SUPPLY VOLTAGE (Y/N)? N	*No change*
EXTERNAL SOURCE RESISTORS (Y/N)? N	*External source resistors not to be used*
INTERNAL VALUE (0,1,10,100) KOHMS ? 100	*Use internal 100k source resistors*
COMMON MODE VOLTAGE (Y/N)? N	*No CMV*
LOW LIMIT IN UA = -.01	*Test limits in μA*
HIGH LIMIT IN UA = .01	
ELIMINATE BINS ? 1	*Failures to Bin 2 or 3 (or higher)*
REPEAT TEST (Y/N)? N	
REPEAT TEST WITH VARIATIONS (Y/N)? Y	*Repeat test with changes*
(TEST : 8) IOS (Y/N)? Y	*Yes – offset current*
CHANGE SUPPLY VOLTAGE (Y/N)? N	*No change*
EXTERNAL SOURCE RESISTORS (Y/N)? N	
INTERNAL VALUE (0,1,10,100) KOHMS ? 100	*Use 100k internal source resistors*
COMMON MODE VOLTAGE (Y/N)? N	*No CMV*
LOW LIMIT IN UA = -.05	*Test limits*
HIGH LIMIT IN UA = .05	
ELIMINATE BINS ? 1,2	*Failed device to Bin 3 (or higher)*
REPEAT TEST (Y/N)? N	*Don't repeat*
REPEAT TEST WITH VARIATIONS (Y/N)? N	
END OF PROGRAM (Y/N)? Y	*End program here (Don't tempt us with further tests.)*

RECALL   STORE   CREATE   DELETE

DEFINE GOOD BINS. ELIMINATE BINS. . .

In the above example, two "good" bins were defined. It is one of the simplest examples of the LTS-2000 component grading system, which perhaps can best be thought of as an elimination matrix containing 49 bins (0 to 48). Bins 1 to 48 can be directly specified by the user; if a component cannot be placed in any of these bins, the system will automatically assign it to bin 0.

To set up the grading system, the user first designates a block of "good" bins anywhere in the range 1–48, usually contiguous, to represent passing components. The number of bins depends on the number of grades into which the device may be assigned and the number of parameters to be tested. A device parameter to be tested may be represented by a bin or a group of bins.

As the user enters the parameters for each test in the program, (s)he must also state that if a component fails a specified test, it cannot be assigned to any of the bins which represent good devices in terms of the parameter being tested. The elimination procedure is repeated for each test in the program. When the device has been exercised through all the tests, the system will automatically grade it into the best bin (lowest bin number) which has not been eliminated.

For example, in the 741J/K test procedure, bins 1 & 2 are defined as "good" bins. A device which passes all tests is graded in bin 1. One which passes tests 2, 4, 6 and 8, but fails 1, 3, 5 *or* 7 is graded into bin 2. And a device which fails 2, 4, 6 and 8 flunks; it is graded into bin 3.

Here is a somewhat more complicated example. Ten devices, A, B, C, D, E, F, G, H, I, J, are to be tested for V_{OS} and I_{OFFSET}. There will be four good grades for each parameter, and two series of four tests are to be performed. For the results of these tests, we arbitrarily define bins 1 to 11 as good bins. We then define the limits, or parameters, for each test, starting with worst-case conditions. By testing for worst-case conditions first, failed components can be identified immediately, avoiding much unnecessary testing. As each limit is defined, the user must also designate which bins are to be eliminated. Here, as Table 1 shows.

Test Number	Failure Condition	Eliminate Bins	Remarks
1	$V_{OS} > 5mV$	1 to 11	Worst case. If device fails, assign it to bin 12. No further test.
2	$V_{OS} > 3mV$	1 to 9	If device fails, cannot be assigned to these bins
3	$V_{OS} > 1.5mV$	1 to 6	Bins 1 to 6 are unavailable to devices that fail this test
4	$V_{OS} > 0.75mV$	1 to 3	Bins 1 to 3 are unavailable to devices that fail this test
5	$I_b^* > 50nA$	1 to 12	Worst case. If device fails, assign it to bin 13. No further test.
6	$I_b^* > 20nA$	1 to 7	If device fails, it cannot be assigned to these bins
7	$I_b^* > 10nA$	1 to 4	Bins 1 to 4 unavailable to failures
8	$I_b^* > 5nA$	1 & 2	Bins 1 & 2 unavailable to failures

Table 1. Tests to be performed.

Assume that the program is written and devices A . . . J are tested. The test results are as shown in Table 2. We will discuss how A and B are classified, show the classifications for devices C, D, E and leave the classifications of F through J to the reader as an easy exercise.

Classification of A: Very simple. It failed Test 1, is rejected to bin 12, and requires no further test.

Classification of B: Since it failed Tests 2 and 6, bins 1–9 are eliminated. It will therefore be assigned to bin 10.

Classification of C,D,E: Bins 7, 4, 1

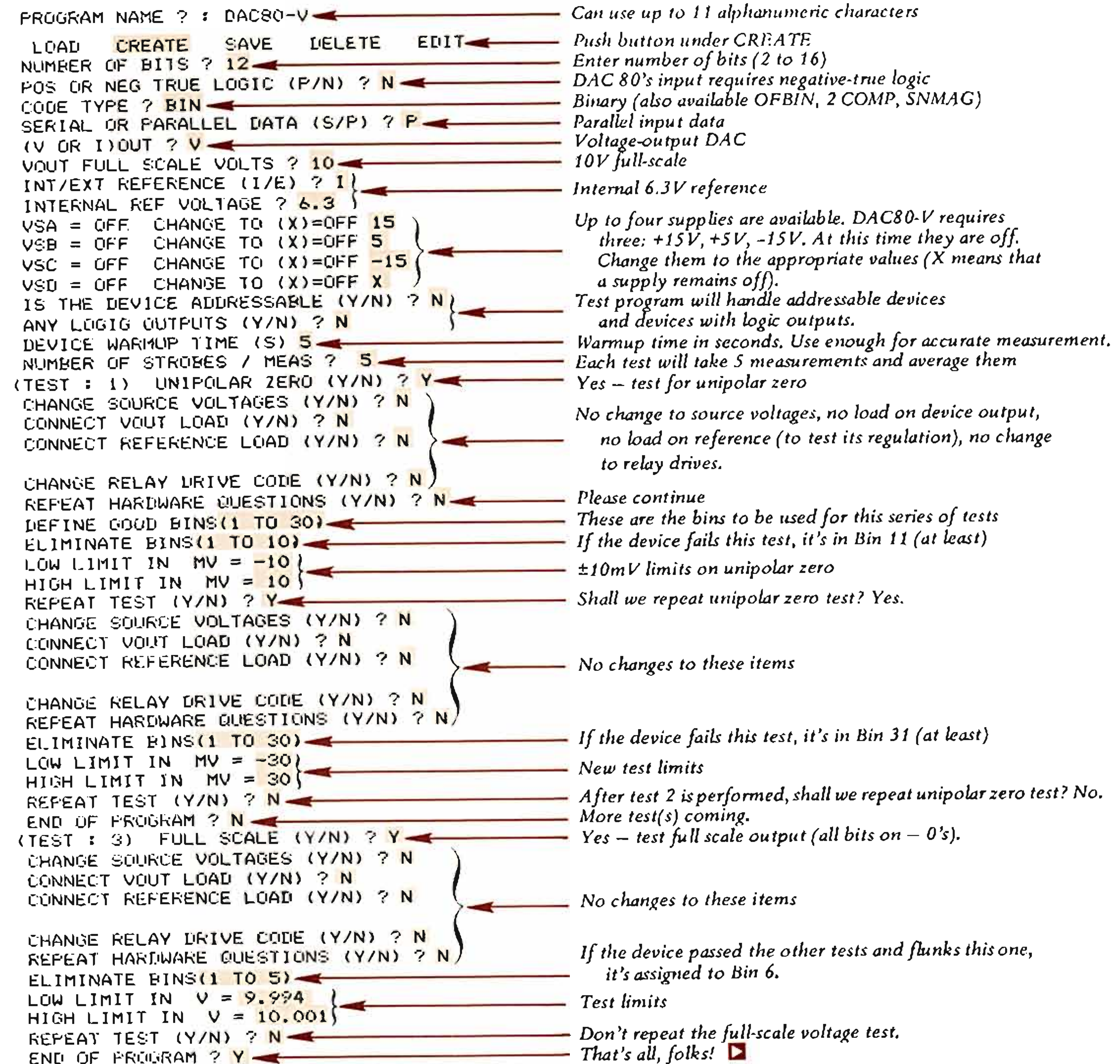
Classification of F,G,H,I,J: See answers in *Potpourri* (p. 19).

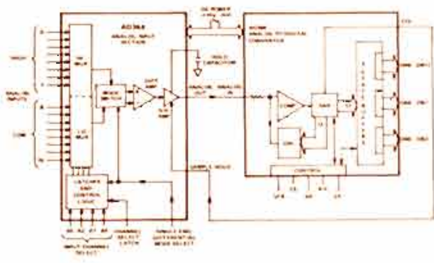
Device	V_{OS}(mV)	I_b(nA)	1	2	3	4	5	6	7	8
A	5.1	60	F	–	–	–	–	–	–	–
B	4.0	25	P	F	F	F	P	F	F	F
C	2.4	15.4	P	P	F	F	P	P	F	F
D	0.8	8.2	P	P	P	F	P	P	P	F
E	0.5	4.1	P	P	P	P	P	P	P	P
F	1.2	2.2	P	P	P	F	P	P	P	P
G	3.3	6.0	P	F	F	F	P	P	P	F
H	4.8	12	P	F	F	F	P	P	F	F
I	6.0	18	F	–	–	–	–	–	–	–
J	2.9	51	P	P	F	F	F	–	–	–

Table 2. Performance of devices' tests (P = Pass, F = Fail).

BRIEF TEST PROGRAM FOR DAC80-V

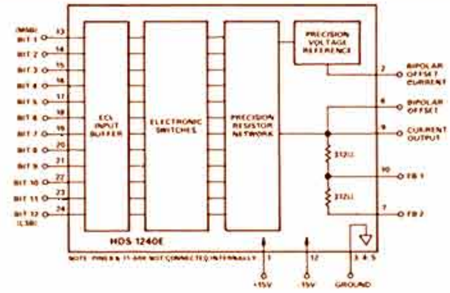
Tests for unipolar zero (±10mV and ±30mV) and full scale (9.994V to 10.001V for all bits on).





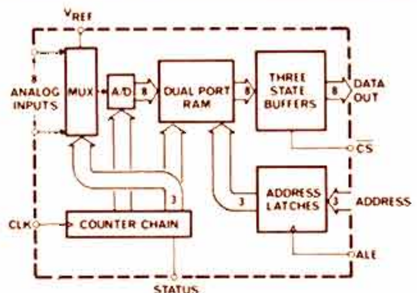
12-BIT 16-CHANNEL DAS

The AD364* is an 8-differential/16-single-ended-channel 12-bit μP-compatible DAS in 2 hermetic DIPs. The analog input section comprises MUXes, differential amplifier, sample-hold, and channel-select logic; the 12-bit μP-compatible ADC is similar to the proven AD574*. Minimum throughput rate for full rated accuracy is 20kHz. Prices from $139.50 (100s).



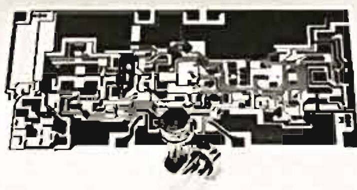
12-BIT 40ns ECL DAC

The HDS-1240E*, a 12-bit high-current (0 to -16mA) hybrid DAC, settles to 12 bits in only 40ns. Designed for random-scan graphic displays, digital VCOs, waveform generation, and military ECM-EW, it replaces such devices as DAC397, DA4000, and ADH-030. The 24-pin hybrid is available in glass/ceramic or hermetic metal packaging. Prices from $149 (1–9).



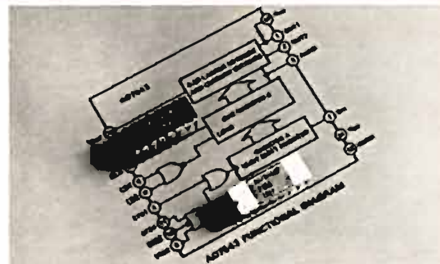
8-BIT 8-CHANNEL MEMORY-DAS

The single-chip CMOS AD7581* continuously scans 8 analog input channels, converts them to digital, and stores the data in bus-addressable RAM. The AD7581 interfaces directly with 8080, 8048, 8085, Z80, 6800, and other microprocessor systems. Data can be read at any time for any channel; on-chip logic provides interleaved DMA. Prices from $13.90 (100s).



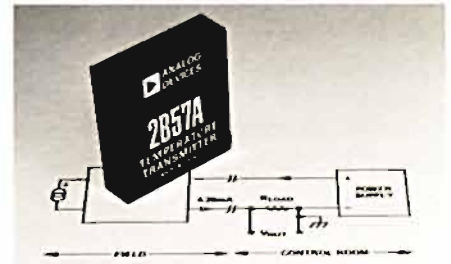
IMPROVED IC OP AMP

The hermetically sealed AD OP-07* is an improved version of the industry standard OP-07 precision op amp. Open-loop gain of 3×10^6 provides increased accuracy in high closed-loop-gain applications (e.g., 0.1% at G = 3000). Its protected inputs have low offset voltage and current, low bias current, and low drift. Its 5 performance grades are priced from $4.55 (100s).



12-BIT SERIAL-INPUT DAC

The AD7543* is a monolithic CMOS 12-bit multiplying DAC in a compact 16-pin DIP. Its double-buffered input permits it to be loaded serially without affecting the analog output until data is strobed in parallel. Serial loading allows a small package, low pin count, and low initial and in-circuit cost for this high-accuracy device. Prices start at $14.25 (100s).



TEMPERATURE TRANSMITTER

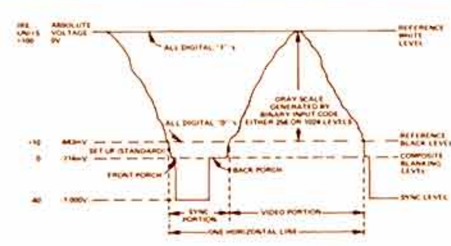
Model 2B57* is a high-performance low-cost -55°C to +150°C-temperature transmitter. Drawing power from the 2-wire output line, it provides excitation and signal conditioning for AD590* or AC2626* IC temperature sensors and has a 4-to-20mA noise-insensitive output current compatible with ISA Standard S.50.1. Prices start at $59 (1–9).

FAST OP AMP AND BUFFER

The ADLH0032 family* are op amps, and the ADLH0033 family* are unity-gain buffer amplifiers, packaged in 12-pin hermetic TO-8 metal cans. Both types are high-slew-rate devices (500/1500V/μs) intended for new applications and for direct replacement of the LH0032/LH0033 families. Industrial and military temperature ranges are available. Prices $29/24 (1–9, substantial quantity discounts available).

8-BIT 9-CHANNEL CMOS ADC

The AD7583* is a 9-channel, addressable 8-bit integrating data-acquisition subsystem on a single CMOS chip in a 40-pin DIP. Operating within spec on a single 12–15V supply, this ratiometric quad-slope device converts in only 4ms, using a small number of external parts. Its 9 addressable buffered channels can be easily expanded to 24. Priced from $17.50 (100s).

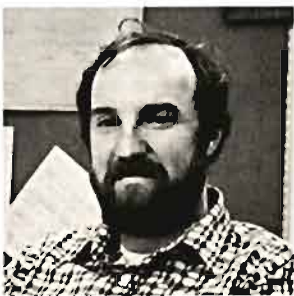


DEGLITCHED 8/10-BIT DACS

The HDD Series* consists of 4 ECL-compatible fast-settling deglitched video DACs packaged in 32-pin DIPs. They offer 10ns settling to 8 bits or 15ns settling to 10 bits, and both versions are available with complete composite video control inputs and compatibility with EIA standards RS-170 & RS-343. Prices start at $159 (1–24).

*For technical data, use the reply card.

THE AUTHORS *(Continued from page 2)*



Gary Sheehan (page 8), a Systems Engineer at ADI's Component Test Systems, designed the DAC Family Board and the software for testing DACs on the LTS-2000. Prior to joining CTS, he has been involved with various stages of IC manufacturing, from IC layout to laser-trimming. Prior to joining Analog Devices, he studied at Northeast Institute and served in the U.S. Navy.

Jan Johnson (page 8), Systems Design Engineer at ADI-CTS, designed the Operational Amplifier Family Board and the software for testing op amps. Earlier, he was involved with ATE systems and product testing at Analog Devices Semiconductor. At present, he is responsible for family-board designs. He studied E.E. at the Worcester Polytechnic Institute.

Tim Wilhelm (page 8), Systems Design Engineer at CTS, has been with Analog Devices since graduating from Northeastern University with a BSEE. As a Test Engineer at ADS, he designed and developed μP-based test systems and configurable environmental chambers for linear-IC production testing. Also responsible for a/d and d/a converter testing of ICs and hybrid circuits, he designed the LTS-2000 ADC Family Test Board.

Steve Castelli (page 14) is Senior Marketing Specialist in charge of marketing operations at ADI Component Test Systems. Earlier, he was Product Marketing Specialist in the ADI Instruments and Systems Group, responsible for various products, from DPMs to interface boards for μCs. Joining us after graduation from Bryant and Stratton, he has worked in Manufacturing and Applications Engineering, as well as Marketing.

Roland Johnson, Publications Manager of CTS, performed the heroic task of stimulating, configuring, and coralling the LTS-2000 articles in this issue, making sure they meshed, and delivering them on time. We are deeply indebted to him. Roland has a B.A. in English and an M.A. in Structural Linguistics. Prior to becoming a technical writer, he was a career officer in the U.S. Army and a teacher. Before joining CTS, he was responsible for MACSYM publications. ▶

ADI Division Fellow Named

JACK MEMISHIAN

Before being named as the newest Analog Devices Division Fellow, Jack Memishian was Senior Staff Engineer in the Systems Component Division. Although his *forte* is products and people, rather than patents and publications, Jack has received two patents and has appeared as an author in these pages. He is currently Chairman of the Analog Devices General Technical Committee and a member of the Strategic Task Force.

Products he has been directly responsible for include the 2B54/55 Isolated Thermocouple/mV Signal Conditioners (that threaten the future of the flying-capacitor multiplexer), the RTI-1200 tribe of memory-mapped I/O boards for microcomputers, and innumerable high-performance a/d converters and DACs, including the fast 14-bit ADC1130/31 and 12-bit DAC1108

Of comparable (or greater) significance are the products that have been and will be developed at the hands of young colleagues, whose professional growth he has fostered through intellectual challenges and generous contributions from his store of ideas, lore, and experience. As one of our engineering managers put it, "He has the faculty to challenge these people to think and to stimulate them to reach beyond their abilities."

Jack received a B.S.E.E. from the Massachusetts Institute of Technology and worked as a Design Engineer at Raytheon before joining Analog Devices some seven years ago.

WHAT IS A DIVISION FELLOW?

Division Fellow is one of the highest levels of technical advancement within the divisions of Analog Devices. Fellows are recognized for their outstanding technical contributions to the company and for having exemplified unusual talents as innovators in their fields; for acting as mentors to young technologists; for having demonstrated leadership in generating new business opportunities; and for having developed valuable industry and academic relationships for the company.

Jack is the third person to be named a Division Fellow in this newly established program, joining A. Paul Brokaw and Barrie Gilbert.* The presentation was made by ADI President and Board Chairman, Ray Stata, who said:

> ". . . the parallel ladder concept, still in its infancy at Analog, is meant to provide opportunity and recognition to individual technical contributors, commensurate with that available to managers, . . . to give engineers a chance to influence the policies and direction of the company, as well as to participate in the material rewards. The technical innovations and superior products for which Analog is known, and to which Jack has made significant contributions, continue to attract and inspire engineers. As we grow larger, we must retain this "magic" and keep the environment stimulating. The maintenance of that environment is high on my list of personal priorities." ▶

*See *Analog Dialogue* 14-1, 1980.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE (Volume 14, No. 2, 1980) . . . *Isolate, Amplify, Multiplex 4+ Channels (All Solid State)*: 2B54, 2B55 . . . *Programmable Cold-Junction Compensator (4 Different TCs)*: 2B56 . . . *Isolated Conversion from Digital to 4-to-20mA* (DAC1423) . . . *Digital Attenuator: 0 to -88.5dB in 1.5dB Steps* (AD7110) . . . *10-Bit 20MHz Video A/D Converter* (MOD-1020) . . . *12-Bit CMOS M-DAC Interfaces Directly with µPs* (AD7542) . . . *Computerized Test System for Linear Devices* (LTS-2000) . . . and these New-Product Briefs: Hybrid 12-Bit S/D Converters (SDC1741/42); 4½-5½ Digit ADC Subsystem on a Chip (AD7555); Fast A/D Converter Modules (MAH-0801, -1001); Data-Acquisition Analog Front End (AD362); Fast Hybrid A/D Converter: 12 Bits in 4µs (AD578); 12-Bit DAC Family (AD370/371); MACSYM: 3 Input Cards — Isolation, Frequency, Bridges; Lowest-Cost Isolators, Stand-Alone and Synchronizable (290A, 292A); Pin-Programmable Hybrid Instrumentation Amplifiers—Binary Gains, 1 to 1024 (AD612/614); µP-Compatible 8-Bit ADC Interfaces Like Memory (AD7574) . . . Application Briefs: *DAC Controls Precision UHF Noise Level* and *Putting the AD558 DACPORT™ on the Bus — Interfacing to µPs with One Easy Chip* . . . New Literature: *1980 Short-Form Guide, MACSYM 2 System Digest*, and new book: *Transducer Interfacing Handbook — a guide to analog signal conditioning* ($14.50) . . . Across the Editor's Desk: *High-Resolution ΔT Measurement, Errors in Sample-Holds* . . . plus Authors, Potpourri, etc. Use the reply card for your free copy, or for information on any of the above items.

WHAT BINS FOR DEVICES F, G, H, I, J? (See page 16) . . . 4, 10, 10, 12, 13.

ARTICLE-REPRINT AND APPLICATION NOTES AVAILABLE . . . "Isolator Stretches the Bandwidth of Two-Transformer Designs," by Bill Morong. *Electronics*, July 3, 1980. All about Model 289 . . . Application Notes: *Interfacing the AD558 DACPORT™ to Microprocessors*, by Doug Grant, and *An Analysis of the Price and Performance of the AD558*, by Goodloe Suttler.

DATA-SHEET UPDATE . . . HDS-1240E Hybrid 12-Bit 40ns ECL DAC, "M" suffixes, has an operating temperature range to +125°C, *up* from 100°C . . . HAS series ADC timing corrections: Data Ready goes low ∼10ns (1 gate delay) before the LSB has settled; time from trailing edge of Encode Command pulse to true state of MSB is about 300ns . . . HTC-0300 has been redesigned to minimize damage caused by static electricity. New specs: Acquisition Time = 170 (200 max)ns, Offset vs. Temp = 40 (75 max) ppm/°C, Bias Current = 15µA max . . . AD534, page 4, first equation: bracket all terms except A . . . AD558 specs: Maximum voltage on the digital inputs (pins 1-10) should be 5.5V (TTL compatible). Do not use high-level CMOS logic voltage . . . AD ADC80-Z will operate with ±12V supplies; tolerance range is ±11.4V to ±16.0V. Logic supply tolerance is +4.75V to +5.25V . . . DAC1423 pin designations are wrong on data sheet C564-9-3/80 but correct in catalog (p. 9-166) . . . Consult your ADI Sales office for more information on any of the items here or in the following sections.

PRODUCT NOTES . . . AD7533 meets or exceeds every AD7520 spec, and it's much lower in price. Other features: Latchproof (no Schottky diode required), lower output capacitance than the competition, end-point linearity spec, *and it's available in quantity!* . . . ADG200/201 switches pass MIL-38510 VZAP test with up to 1000V ZAP! . . . AD501 replacements: AD511A/B/C replace AD501A/B/C (plastic-end-lead mini package); ADP511A/B/C replace ADP501A/B/C (plastic-bottom-lead mini package; ADM501/506A,B,C replace ADM501 A,B,C (12-lead TO-8 metal can); GBW = 1MHz . . . Chassis-mount power supplies: barrier strips are ½" longer for improved reliability and safety . . . AC2626 probe version of AD590 temperature sensor withstands 7500psi (15 min) pressure testing; for information, consult your ADI Sales office . . . 2B54/55 4-Channel Thermocouple/mV Signal Conditioners and 2B56 Cold-Junction Compensator: two mounting cards are available with all adjustment pots, address-decoding circuitry, and cold-junction sensor on-board. AC1215 has screw terminals for thermocouple inputs, AC1216 has a finger-type edge connector.

APPLICATION NOTES . . . MAS Series a/d converters can be short-cycled: 120ns/bit for MAS-1202, 115ns/bit for MAS-1001, and 90ns/bit for MAS-0801 . . . AD7525 Digital Pot, for best results when used with thumbwheel switches: pulldowns should be used to draw current through the switch contacts in the Logic 0 position. This tends to prevent poisoning of the contact surfaces under "dry circuit" conditions . . . Socket information for AD515, AD545, AD362, AD363, AD364 AIS, AD ADC80, AD5200, AD572, and AD578 is available from your ADI Sales office . . . AD565/566 grounding: the grounds must be tied together at the power ground pin.

PRICES . . . AD7533JN prices have been drastically reduced. For example, the new price in 100s is $4.00, down from $6.00 . . . MIL versions of the AD7542 are available, starting at $37.85 in 100s for the MIL-temp-range AD7542SD. Mil/883B screeening is available for all types, starting at $22.25 in 100s for the industrial-grade AD7542AD/883B. Consult the ADI Sales Office for prices of other types or in other quantities.

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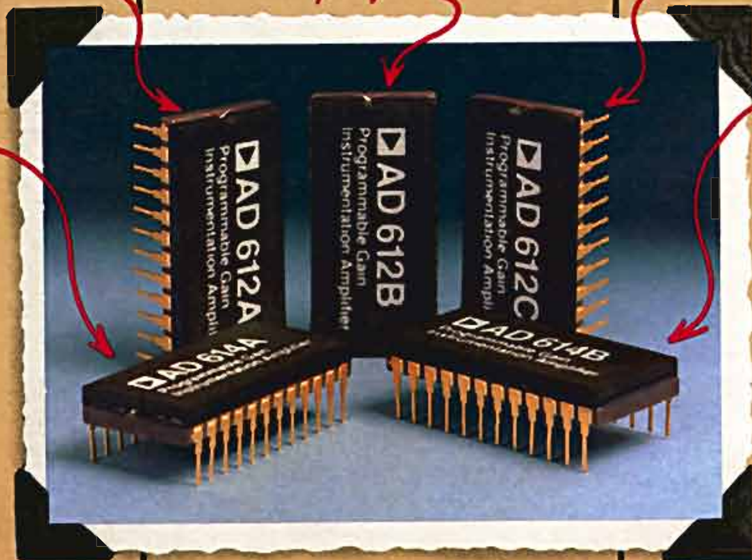

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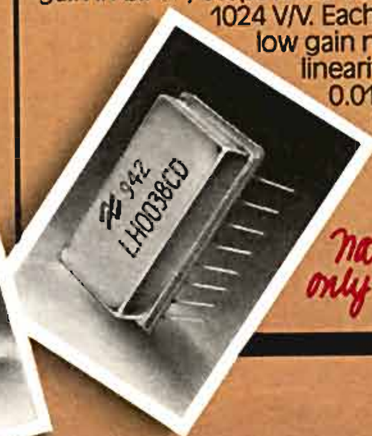

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